Abstract of the Disclosure:

A test circuit for testing a memory circuit has a data input line for providing test data and a comparator unit. The comparator unit is connected to the data input line and to the memory circuit for comparing the test data written into the memory circuit with the test data read from the memory area. The data input line is connected to the memory circuit via a data change circuit. The data change circuit is controllable depending on a result of a comparison in the comparator unit such that when an error occurs, subsequent test data can be written in an altered manner to the memory circuit.

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